Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

Claims 1-9: (Canceled)

10. (New) A method for producing a silicon epitaxial wafer, comprising the steps of:

a sub-epitaxial layer forming step of forming a sub-epitaxial layer on a main surface of a silicon single crystal substrate to which boron, arsenic or phosphorus is added as a dopant, and

a main epitaxial layer forming step of forming a main epitaxial layer on the sub-epitaxial layer, the sub-epitaxial layer forming step and the main epitaxial layer forming step being performed in this order to form a silicon epitaxial layer having the main epitaxial layer and the sub-epitaxial layer on the main surface of the silicon single crystal substrate,

wherein as the silicon single crystal substrate, a substrate having a rear surface on which a silicon oxide film for auto-doping prevention is formed, is used, and

a hydrofluoric acid treating step of dipping the silicon single crystal substrate in a hydrofluoric acid to perform wet etching of an oxide film formed on the main surface of the silicon single crystal substrate while the silicon oxide film for auto-doping prevention is allowed to remain, and

a baking step of performing dry etching of a natural oxide film formed on the main surface of the silicon single crystal substrate in a hydrogen gas atmosphere while the silicon single crystal substrate is heated to a temperature lower than a growth temperature of the main epitaxial layer, are performed in this order and then the sub-epitaxial layer forming step is performed.

11. (New) The method as claimed in claim 10, wherein the baking step is performed while the silicon single crystal substrate is heated to a temperature of 950°C or less.

12. (New) The method as claimed in claim 10, wherein a thickness of the sub-epitaxial layer is formed to be less than 0.5 μm.

13. (New) The method as claimed in claim 11, wherein a thickness of the sub-epitaxial layer is formed to be less than 0.5 μm.

14. (New) The method as claimed in claim 11, wherein the sub-epitaxial layer forming step is performed while a temperature of the silicon single crystal substrate is raised.

15. (New) The method as claimed in claim 13, wherein the sub-epitaxial layer forming step is performed while a temperature of the silicon single crystal substrate is raised.

16. (New) The method as claimed in claim 10, wherein a time of exposing the silicon single crystal substrate to air between the hydrofluoric acid treating step and the baking step is set within 60 minutes.

17. (New) The method as claimed in claim 12, wherein a time of exposing the silicon single crystal substrate to air between the hydrofluoric acid treating step and the baking step is set within 60 minutes.

18. (New) The method as claimed in claim 14, wherein a time of exposing the silicon single crystal substrate to air between the hydrofluoric acid treating step and the baking step is set within 60 minutes.

19. (New) The method as claimed in claim 15, wherein a time of exposing the silicon single crystal substrate to air between the hydrofluoric acid treating step and the baking step is set within 60 minutes.

20. (New) The method as claimed in claim 14, wherein the main epitaxial layer forming step is performed while the silicon single crystal substrate is heated to a temperature of 900 to 1200°C.

21. (New) The method as claimed in claim 18, wherein the main epitaxial layer forming step is performed while the silicon single crystal substrate is heated to a temperature of 900 to 1200°C.

22. (New) The method as claimed in claim 15, wherein the main epitaxial layer forming step is performed while the silicon single crystal substrate is heated to a temperature of 900 to 1200°C.

23. (New) The method as claimed in claim 19, wherein the main epitaxial layer forming step is performed while the silicon single crystal substrate is heated to a temperature of 900 to 1200°C.

24. (New) The method as claimed in claim 16, wherein resistivity of the main surface of the main epitaxial layer is set to not less than 20 times that of the silicon single crystal substrate.

25. (New) The method as claimed in claim 17, wherein resistivity of the main surface of the main epitaxial layer is set to not less than 20 times that of the silicon single crystal substrate.

26. (New) The method as claimed in claim 20, wherein resistivity of the main surface of the main epitaxial layer is set to not less than 20 times that of the silicon single crystal substrate.

27. (New) The method as claimed in claim 21, wherein resistivity of the main surface of the main epitaxial layer is set to not less than 20 times that of the silicon single crystal substrate.

28. (New) The method as claimed in claim 22, wherein resistivity of the main surface of the main epitaxial layer is set to not less than 20 times that of the silicon single crystal substrate.

29. (New) The method as claimed in claim 23, wherein resistivity of the main surface of the main epitaxial layer is set to not less than 20 times that of the silicon single crystal substrate.

30. (New) The method as claimed in claim 24, wherein a substrate having a dopant concentration of 1×10^{19} /cm^3 or more is used as the silicon single crystal substrate.

31. (New) The method as claimed in claim 25, wherein a substrate having a dopant concentration of 1×10^{19} /cm^3 or more is used as the silicon single crystal substrate.

32. (New) The method as claimed in claim 26, wherein a substrate having a dopant concentration of 1×10^{19} /cm^3 or more is used as the silicon single crystal substrate.

33. (New) The method as claimed in claim 29, wherein a substrate having a dopant concentration of 1×10^{19} /cm^3 or more is used as the silicon single crystal substrate.

34. (New) A method for producing a silicon epitaxial wafer, comprising the steps of:

using a silicon single crystal substrate to which boron, arsenic or phosphorus is added as a dopant in a concentration of 1×10^{19} /cm^3 or more, the silicon single crystal substrate having a rear surface on which a silicon oxide film for auto-doping prevention is formed,

a hydrofluoric acid treating step of dipping the silicon single crystal substrate in a hydrofluoric acid to perform wet etching of an oxide film formed on a main surface of the silicon single crystal substrate while the silicon oxide film for auto-doping prevention is allowed to remain,

a baking step of inputting the silicon single crystal substrate into a vapor phase growth apparatus after the hydrofluoric acid treating step while a time of exposing the silicon single crystal substrate to air is set within 60 minutes, and performing dry etching of a natural oxide film formed on the main surface of the silicon single crystal substrate in a hydrogen gas

atmosphere while the silicon single crystal substrate is heated to a temperature of 950°C or less,

a sub-epitaxial layer forming step of performing a vapor phase growth of a sub-epitaxial layer having a thickness of less than 0.5 μm on the main surface of the silicon single crystal substrate while a temperature of the silicon single crystal substrate is raised toward a vapor phase growth temperature of a main epitaxial layer immediately after the baking step is finished, and

a main epitaxial layer forming step of performing a vapor phase growth of the main epitaxial layer with the main surface having resistivity which is not less than 20 times that of the silicon single crystal substrate, on the sub-epitaxial layer.